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MEGIC-00-001

December 14, 2000

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

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Subject: Serial No. 09/684,519 10/10/00

Jin-Yuan Lee

A THERMALLY COMPLIANT PCB SUBSTRATE FOR THE APPLICATION OF CHIP SCALE PACKAGES

Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

U.S. Patent 6,031,282 to Jones et al., "High Performance Integrated Circuit Chip Package", discloses an IC package with an elastomer on a PCB and die pads.

U.S. Patent 5,889,652 to Turturro, "C4-GT Stand Off Rigid Flex Interposer", discloses a PCB and a substrate with an elastomer therebetween.

U.S. Patent 6,041,495 to Yoon et al., "Method of Manufacturing a Circuit Board Having Metal Bumps and a Semiconductor Device Package Comprising the Same", discloses a PCB with an elastomer and chip mount.

U.S. Patent 5,990,545 to Schueller et al., "Chip Scale Ball Grid Array for Integrated Circuit Package", discloses a SCBGA with a PCB and direct chip attach with an elastomer to compensate for the thermal mismatch of the PCB and the die.

DiStefano et al., "Designing a Modular Chip-Scale Package Assembly Line", Circuit Assembly, March 1977, (pages not numbered), focuses on the Chip Scale Package (CSP) and provides methods and procedures for relatively easy assembly of CSP's.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761